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# A Double Phase-Shift Control Strategy for A Full-Bridge Three-Level DC/DC Converter

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**Abstract**—In this paper, a double phase-shift control strategy is proposed for a full-bridge three-level (FBTL) dc/dc converter in dc distribution systems with the medium dc bus voltage. The proposed control strategy can effectively reduce the voltage change rate  $dv/dt$  and voltage stress on the transformer, which means that the reliability and EMC of the FBTL dc/dc converter can be improved. The operation principle and performances of the proposed control strategy is analyzed in detail. Finally, the simulation results are presented to verify the proposed control strategy.

**Keywords**—Full-bridge; medium dc bus voltage; phase-shift; three-level dc/dc converter.

## I. INTRODUCTION

Dc distribution systems and dc micro-grids have been proposed as promising solutions for future smart-grid systems because of their clear merits, such as no reactive power, no frequency stability, high conversion efficiency, and easy system control [1-3]. Furthermore, dc-based data centers and residential systems have been increasingly developed recently [4], [5]. The performance of dc systems highly depends on dc/dc converters, which are responsible for delivering power and changing voltage levels in dc grids. Generally, a high or medium dc voltage is needed for the dc distribution systems and micro-grids to reduce the transmission losses and increase the power delivery capability. Therefore, the scientific researches on the medium voltage dc/dc converters with high performance and high reliability are quite desired.

The three-level (TL) dc/dc converter is attractive for the dc distribution grids with the medium dc bus voltage [6]. So far, a number of studies have been done on TL based dc/dc converters [7-15]. In [7], a zero voltage and zero current switching half-bridge (HB) TL dc/dc converter was proposed, in which a flying capacitor in the primary side is added to make the phase-shift control strategy applied to TL dc/dc converter. Based on [7], an auxiliary circuit is added in the secondary side to reduce the circulating current for improving the efficiency [8]. In [9], a new four-switch HB zero-voltage-switching (ZVS) TL dc/dc converter was proposed, which features with simple and compact circuit structure by adding one additional wire between the mid-points of the input capacitors and switching pairs but removing two clamped diodes. The new solutions to achieve the wide range soft-

switching are discussed in [10] based on the circuit structure of the four-switch HBTL converter, in which four kinds of new pulse-wide modulation PWM TL dc/dc converters are proposed for the industrial application. A secondary-side phase-shift-controlled ZVS dc/dc converter with wide voltage gain and a three-phase dc/dc converter with low voltage stress on the power switches are proposed in [11] and [12] for the high voltage applications. Two control strategies which are chopping phase-shift (CPS) control and double phase-shift (DPS) control respectively are presented in [13] and [14] for the isolated full-bridge three-level (FBTL) dc/dc converter. But the two control strategies both cause high voltage change rate  $dv/dt$  on the primary side voltage of the transformer, which would cause large electromagnetic interference (EMI) and thus lead them not suitable for the medium or high voltage applications. In [15], an improved FBTL dc/dc converter with a voltage balance control strategy of the input capacitors is proposed to reduce the  $dv/dt$ . However, a passive filter is inserted into the primary side of the transformer, which would result in reducing the voltage conversion rate and efficiency.

In this paper, a double phase-shift control strategy is proposed for the FBTL dc/dc converter applied to the dc grids with the medium dc bus voltage. Comparing with the conventional control strategy, the proposed control strategy can effectively reduce the voltage change rate  $dv/dt$  and voltage stress on the transformer, and thus improve both EMI and reliability of the converter. The operation principle and performance of the proposed control strategy are analyzed in detail. Finally, the simulation results are shown to validate the proposed double phase-shift control strategy.

This paper is organized as follows. Section II analyzes the operation principle of the proposed double phase-shift control strategy in detail. Section III analyzes the characteristics and performances of the FBTL dc/dc converter under the proposed control strategy theoretically. Section IV presents the simulation results to verify the theoretical analysis. Finally, the main contributions of this paper are summarized in Section V.

## II. OPERATION PRINCIPLE

Fig. 1 shows the circuit structure of the FBTL dc/dc converter and main operation waveforms under the proposed double phase-shift control strategy.  $C_{i1}$  and  $C_{i2}$  are two input capacitors which split the input voltage  $V_{in}$  into  $V_1$  and  $V_2$ .  $S_1$ -

$S_8$  and  $D_1$ - $D_8$  are power switches and their body diodes.  $C_1$ - $C_8$  are junction capacitors.  $C_{s1}$  and  $C_{s2}$  are two flying capacitors.  $D_9$ - $D_{12}$  are four clamped diodes.  $L_r$  is leakage inductance of the transformer  $T_r$ . In the secondary side, there are four rectifier diodes  $D_{r1}$ - $D_{r4}$ , an output filter  $L_o$ , and an output filter capacitor  $C_o$ . In Fig. 1(a), the input voltage is  $V_{in}$ ; the voltage between point a and b is  $V_{ab}$ ; the primary current of the transformer is  $i_p$ ; the current through output filter inductor is  $i_{L_o}$ ; the output current and voltage are  $I_o$  and  $V_o$ ; the turns ratio of the transformer  $T_r$  is  $n$ . In Fig. 1(b),  $d_{rv1}$ - $d_{rv8}$  are driving signals of the switches  $S_1$ - $S_8$ ;  $\alpha_1$  and  $\alpha_2$  are two time delays.

For simplifying the analysis, some assumptions are made: 1) all the capacitors and inductances are ideal; 2) all the power devices and the diodes are ideal; 3) the power switches  $S_1$ - $S_8$  have the same parasitic capacitors, which means that  $C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C_7 = C_8 = C_j$ ; 4) the input divided capacitors  $C_{i1}$  and  $C_{i2}$  are large enough to be regarded as two voltage sources with the value of  $V_{in}/2$ ; 5) the two flying capacitors  $C_{s1}$  and  $C_{s2}$  are large enough to be regarded as two voltage sources with the values of  $V_{in}/2$ ; and 6) the output filter inductance  $L_o$  is large enough to be regarded as a constant current source during a switching period.

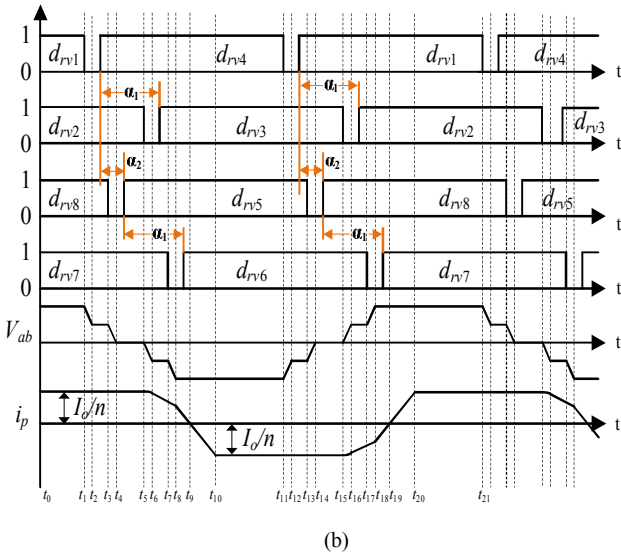
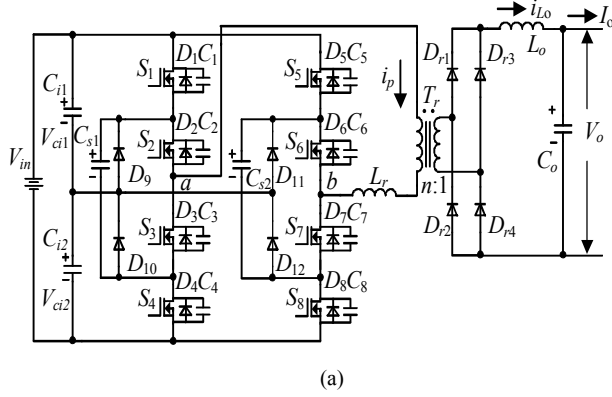


Fig. 1. Circuit structure and main operation waveforms. (a) Circuit Structure. (b) Main waveforms under the proposed control strategy

Fig. 2 shows the equivalent circuits under the proposed double phase-shift control strategy.

Stage 1 [ $t_0 - t_1$ ]: During this period,  $S_1$ ,  $S_2$ ,  $S_7$ , and  $S_8$  are all on-state, so  $V_{ab}$  equals  $V_{in}$  and the input power transfers to the load from  $D_{r1}$  and  $D_{r4}$ . During this stage, the primary current of the transformer  $i_p$  is  $I_o/n$ .

Stage 2 [ $t_1 - t_2$ ]: At  $t_1$ ,  $S_1$  is turned off. Then  $I_o$  is reflected to the primary side, which means  $i_p$  is still  $I_o/n$  to charge  $C_1$  and discharge  $C_4$  via  $C_{s1}$ . Therefore,  $V_{c1}$  increases and  $V_{c4}$  decreases linearly.

$$V_{c1}(t) = \frac{I_o}{2 \cdot n \cdot C_j} (t - t_1) \quad (1)$$

$$V_{c4}(t) = \frac{V_{in}}{2} - \frac{I_o}{2 \cdot n \cdot C_j} (t - t_1) \quad (2)$$

The duration of the stage 2 is:

$$t_2 - t_1 = \frac{n \cdot V_{in} \cdot C_j}{I_o} \quad (3)$$

Stage 3 [ $t_2 - t_3$ ]: At  $t_2$ ,  $V_{c1}$  increases to  $V_{in}/2$  and  $D_9$  conducts, which clamps  $V_{c4}$  at 0 V. Therefore,  $S_4$  can be turned on with zero-voltage. During this stage,  $V_{ab}$  is  $V_{in}/2$  and  $i_p$  remains  $I_o/n$ .

Stage 4 [ $t_3 - t_4$ ]: At  $t_3$ ,  $S_8$  is turned off;  $i_p$  maintains at  $I_o/n$  to charge  $C_8$  and discharge  $C_5$  via  $C_{s2}$ .  $V_{c8}$  increases and  $V_{c5}$  decreases linearly.

$$V_{c8}(t) = \frac{I_o}{2 \cdot n \cdot C_j} (t - t_3) \quad (4)$$

$$V_{c5}(t) = \frac{V_{in}}{2} - \frac{I_o}{2 \cdot n \cdot C_j} (t - t_3) \quad (5)$$

The duration of the stage 4 is

$$t_4 - t_3 = \frac{n \cdot V_{in} \cdot C_j}{I_o} \quad (6)$$

Stage 5 [ $t_4 - t_5$ ]: At  $t_4$ ,  $V_{c8}$  increases to  $V_{in}/2$  and  $D_{12}$  conducts, which clamps the voltages of  $S_5$  at 0 V. So  $S_5$  can be turned on with zero-voltage. During this stage,  $V_{ab}$  is 0 V and  $i_p$  is  $I_o/n$ .

Stage 6 [ $t_5 - t_6$ ]: At  $t_5$ ,  $S_2$  is turned off. Then  $C_2$  is charged and  $C_3$  is discharged;  $V_{ab}$  changes to negative. The current  $i_p$  starts to decrease and is not enough to provide  $I_o$ , so  $D_{r1}$ ,  $D_{r2}$ ,  $D_{r3}$ , and  $D_{r4}$  conduct simultaneously, which clamps both the primary and secondary voltage at 0 V. Thus the voltage of  $V_{ab}$  is fully applied on  $L_r$ . During this stage,  $L_r$  resonates with  $C_2$  and  $C_3$ .

$$i_p(t) = \frac{I_o}{n} \cdot \cos \omega_r (t - t_5) \quad (7)$$

$$V_{c2}(t) = \frac{I_o}{n} \cdot Z_r \cdot \sin \omega_r (t - t_5) \quad (8)$$

$$V_{c3}(t) = \frac{V_{in}}{2} - \frac{I_o}{n} \cdot Z_r \cdot \sin \omega_r (t - t_5) \quad (9)$$

where  $Z_r = \sqrt{L_r / (2 \cdot C_j)}$ ,  $\omega_r = \sqrt{1 / (2 \cdot C_j \cdot L_r)}$ .

The duration of the stage 6 is:

$$t_6 - t_5 = (\arcsin \frac{V_{in} \cdot n}{2 \cdot I_o \cdot Z_r}) / \omega_r \quad (10)$$

$$i_p(t_6) = \frac{I_o}{n} \cdot \cos \omega_r(t_6 - t_5) \quad (11)$$

Stage 7 [ $t_6 - t_7$ ]: At  $t_6$ ,  $V_{c2}$  increases to  $V_{in}/2$ ;  $V_{c3}$  decreases to 0 V;  $V_{ab}$  decreases to  $-V_{in}/2$ . Then  $D_3$  conducts, which clamps the voltage of  $S_3$  at 0 V, so  $S_3$  can be turned on with zero-voltage. Because  $D_{r1}$ ,  $D_{r2}$ ,  $D_{r3}$ , and  $D_{r4}$  keep conducting,  $-V_{in}/2$  is fully applied on  $L_r$ , so  $i_p$  decays linearly:

$$i_p(t) = i_p(t_6) - \frac{V_{in}}{2 \cdot L_r}(t - t_6) \quad (12)$$

At  $t_7$ , the primary current of transformer is

$$i_p(t_7) = i_p(t_6) - \frac{V_{in}}{2 \cdot L_r}(t_7 - t_6) \quad (13)$$

Stage 8 [ $t_7 - t_8$ ]: At  $t_7$ ,  $S_7$  is turned off,  $C_7$  is charged and  $C_6$  is discharged;  $V_{ab}$  changes from  $-V_{in}/2$  to  $-V_{in}$ . During this stage,  $i_p$  continues to decrease and  $D_{r1}$ ,  $D_{r2}$ ,  $D_{r3}$ , and  $D_{r4}$  remain conducting, which clamps both the primary and secondary voltage at 0 V. During this stage,  $L_r$  resonates with  $C_6$  and  $C_7$ , so the voltages on  $C_6$  and  $C_7$  can be given by

$$i_p(t) = i_p(t_7) \cdot \cos \omega_r(t - t_7) \quad (14)$$

$$V_{c7}(t) = i_p(t_7) \cdot Z_r \cdot \sin \omega_r(t - t_7) \quad (15)$$

$$V_{c6}(t) = \frac{V_{in}}{2} - i_p(t_7) \cdot Z_r \cdot \sin \omega_r(t - t_7) \quad (16)$$

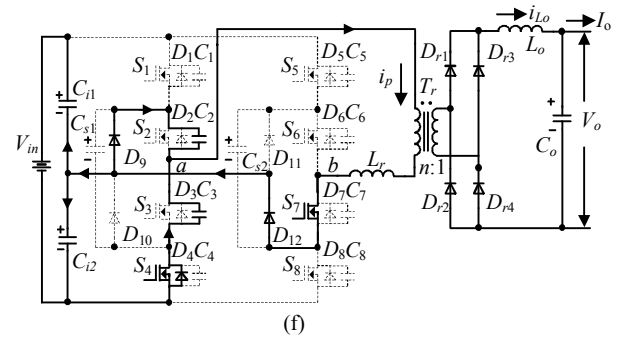
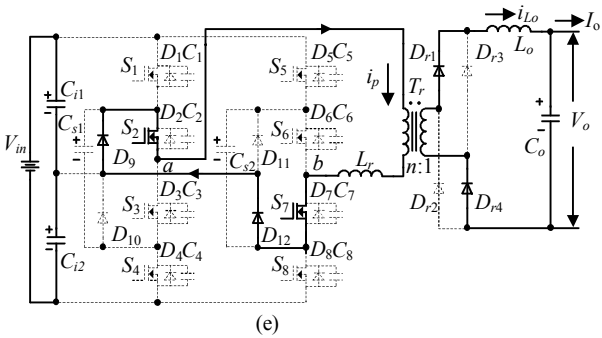
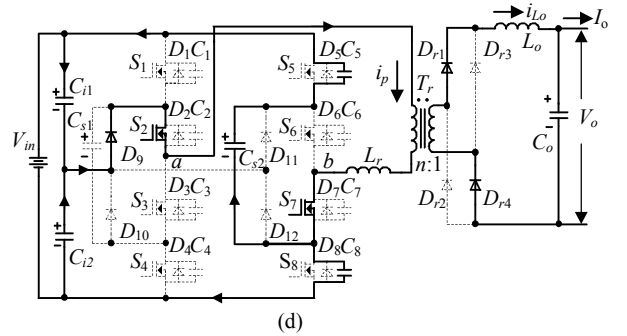
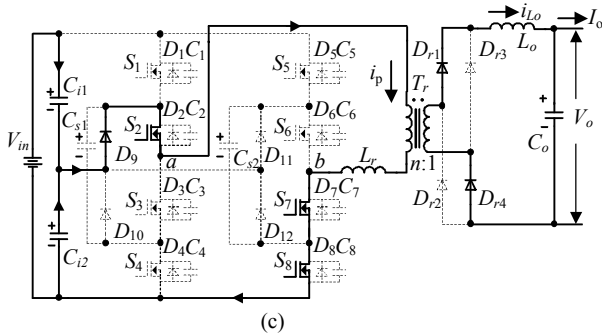
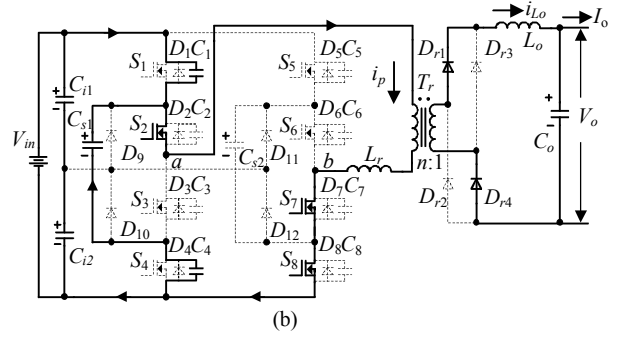
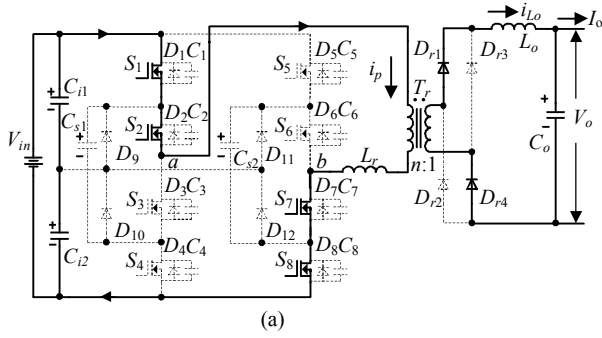
Stage 9 [ $t_8 - t_9$ ]: At  $t_8$ , the voltage of  $S_7$  is  $V_{in}/2$ ,  $D_6$  conducts, which clamps the voltage of  $S_6$  at 0 V, therefore  $S_6$  can be turned on with zero-voltage.  $D_{r1}$ ,  $D_{r2}$ ,  $D_{r3}$ , and  $D_{r4}$  still keep conducting, thus the voltage on  $L_r$  is  $-V_{in}$  and  $i_p$  decreases linearly:

$$i_p(t) = i_p(t_8) - \frac{V_{in}}{L_r}(t - t_8) \quad (17)$$

Stage 10 [ $t_9 - t_{10}$ ]: At  $t_9$ ,  $i_p$  decreases to 0 A, which means the current direction of  $i_p$  would change. The voltage on  $L_r$  remains  $-V_{in}$ , so  $i_p$  still decreases linearly.

Stage 11 [ $t_{10} - t_{11}$ ]: At  $t_{10}$ ,  $i_p$  reaches to the negative reflected output current whose value is  $-I_o/n$ . Then  $D_{r1}$  and  $D_{r4}$  are turned off, and the input power transfers to load from  $D_{r2}$  and  $D_{r3}$ .

At  $t_{11}$ ,  $S_4$  is turned off. The second half cycle [ $t_{11} - t_{21}$ ] starts. The following analysis is similar to the first half cycle [ $t_1 - t_{11}$ ], which is not repeated here.



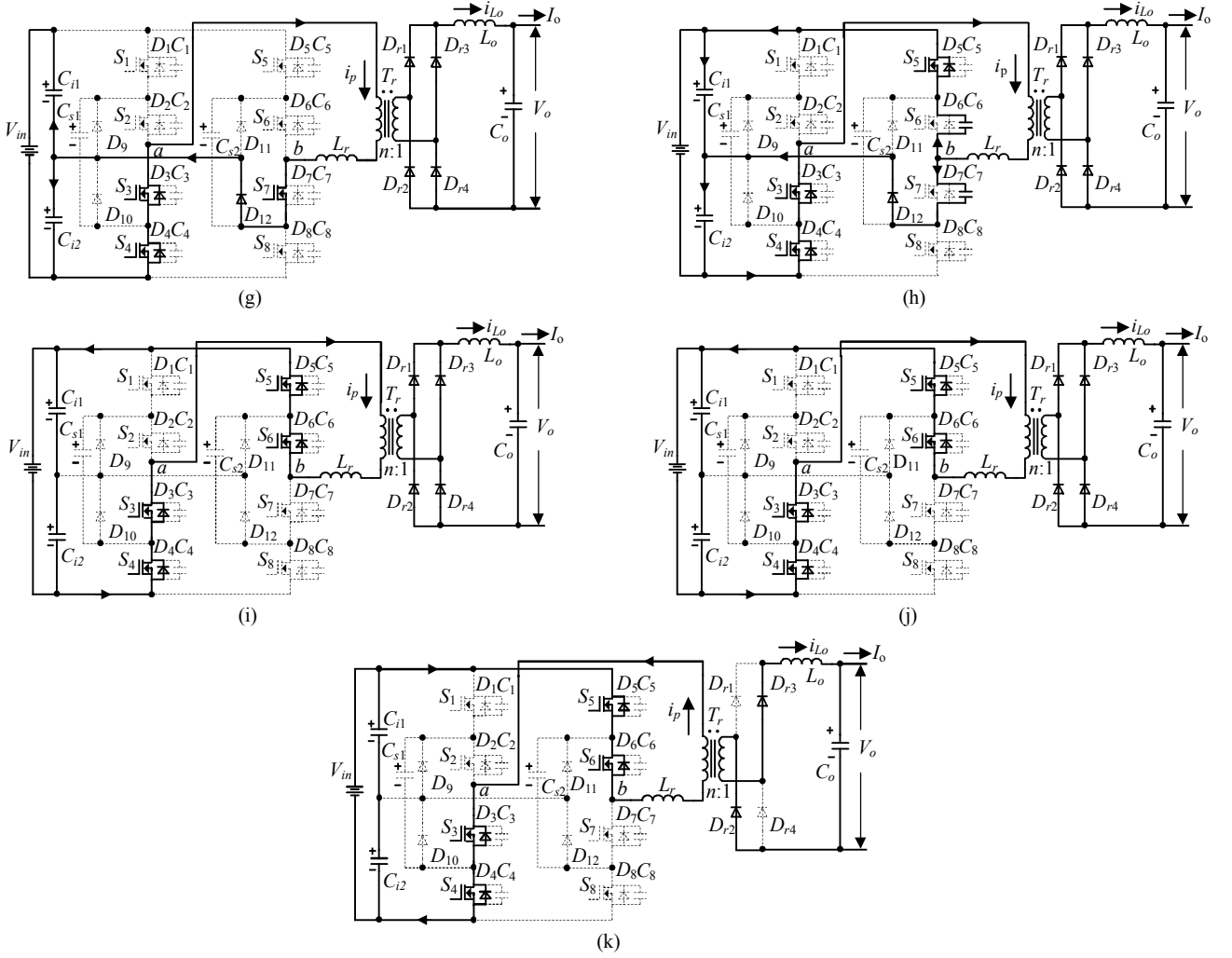


Fig. 2. Equivalent circuits. (a)  $[t_0-t_1]$ . (b)  $[t_1-t_2]$ . (c)  $[t_2-t_3]$ . (d)  $[t_3-t_4]$ . (e)  $[t_4-t_5]$ . (f)  $[t_5-t_6]$ . (g)  $[t_6-t_7]$ . (h)  $[t_7-t_8]$ . (i)  $[t_8-t_9]$ . (j)  $[t_9-t_{10}]$ . (k)  $[t_{10}-t_{11}]$

### III. CHARACTERISTIC AND PERFORMANCES

In this section, the characteristic and performances of the FBTL dc/dc converter under the proposed control strategy are analyzed in detail.

#### A. Voltage Stress of Power Switches

From the above analysis, all the power switches of the FBTL converter only need to withstand half of the input voltage.

#### B. Duty Cycle Loss

$[t_5 - t_{10}]$  and  $[t_{15} - t_{20}]$  are time intervals of duty cycle losses as shown in Fig. 1(b), in which the primary current of the transformer  $i_p$  changes from the positive (or negative) direction to the negative (or positive) reflected output filter inductor current. The two time intervals are the same and can be given by

$$t_{10} - t_5 = t_{20} - t_{15} = \frac{\alpha_2}{2} + \frac{2 \cdot L_r \cdot I_o}{n \cdot V_{in}} \quad (18)$$

According to (18), the duty cycle loss in one switching cycle namely  $D_{loss}$  can be calculated by

$$D_{loss} = \frac{(t_{10} - t_5) + (t_{20} - t_{15})}{T_s} = \frac{\alpha_2}{T_s} + \frac{4 \cdot L_r \cdot I_o}{n \cdot V_{in} \cdot T_s} \quad (19)$$

#### C. Conditions of ZVS Achievement for Power Switches

##### 1) Leading Switches

The zero-voltage switch-on of the leading switches  $S_1$ ,  $S_4$ ,  $S_5$ , and  $S_8$  are mainly decided by the reflected current from the output filter inductance. Normally, the output filter inductance is quite large enough to let the leading switches achieve zero-voltage switch-on even at light load. For instance, in order to ensure the zero-voltage switch-on of the leading switch  $S_4$ , the energy  $E_1$  is needed to fully discharge the parasitic capacitor  $C_4$  and charge the intrinsic capacitor  $C_1$ . The expression of  $E_1$  can be given by

$$E_1 \geq \frac{1}{2} \cdot C_1 \cdot \left(\frac{V_{in}}{2}\right)^2 + \frac{1}{2} \cdot C_4 \cdot \left(\frac{V_{in}}{2}\right)^2 = \frac{1}{4} \cdot C_j \cdot V_{in}^2 \quad (20)$$

##### 2) Lagging Switches

Only the energy of the leakage inductance (and resonant inductance if adding in the circuit) is used for realizing the zero-voltage switch-on of lagging switches  $S_2$ ,  $S_3$ ,  $S_6$ , and  $S_7$ . Therefore, in order to achieve the zero-voltage switch-on, the following equation (21) should be satisfied.

$$\frac{1}{2}L_r \cdot \left(\frac{I_o}{n}\right)^2 \geq \frac{1}{2}C_j \cdot V_{in}^2 + \frac{V_{in} \cdot \alpha_2}{2} \cdot \sqrt{\left(\frac{I_o}{n}\right)^2 - \frac{C_j}{2L_r} \cdot V_{in}^2} - \frac{V_{in}^2}{8L_r} \cdot \alpha_2^2 \quad (21)$$

#### D. Output Characteristic

The output voltage  $V_o$  can be calculated by

$$\begin{aligned} V_o &= \frac{V_{in}}{n} \cdot \left(1 - \frac{2 \cdot \alpha_1}{T_s} - D_{loss}\right) + \frac{V_{in}}{2 \cdot n} \cdot \frac{4 \cdot \alpha_2}{T_s} \\ &= \frac{V_{in}}{n} \cdot \left(1 - \frac{2 \cdot \alpha_1}{T_s} + \frac{\alpha_2}{T_s} - \frac{4 \cdot L_r \cdot I_o}{n \cdot V_{in} \cdot T_s}\right) \end{aligned} \quad (22)$$

#### IV. SIMULATION VERIFICATION

In order to verify the proposed double phase-shift control strategy, a simulation model is built in PLECS, whose parameters are listed in Appendix.

In the simulation model,  $\alpha_2$  is set as  $5\mu s$  and the output voltage  $V_o$  is controlled by adjusting  $\alpha_1$ . Fig. 3 shows the simulation results including voltages  $V_{in}$ ,  $V_{ab}$ ,  $V_o$  and currents  $i_p$ ,  $i_o$  under the proposed control strategy. Fig. 4 shows the comparison results between the control strategy in [14] and the proposed control strategy. From Fig. 4, it can be observed that the voltage change rate  $dv/dt$  of  $V_{ab}$  is effectively reduced by utilizing the proposed double phase-shift control strategy, which means the voltage stress on the transformer is reduced, as marked in Fig. 4(b).

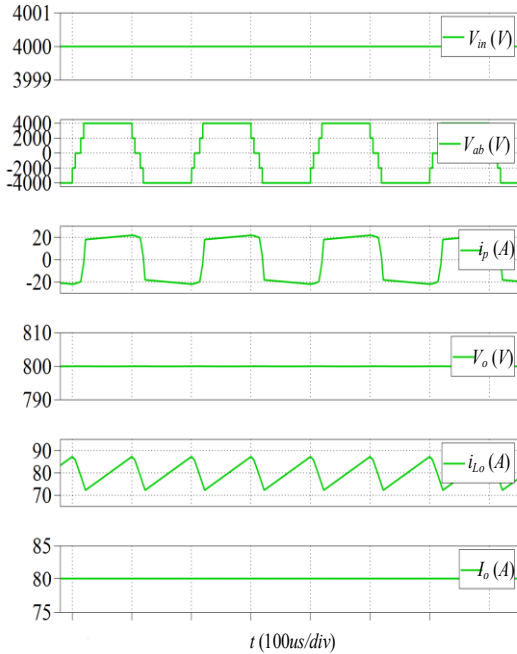
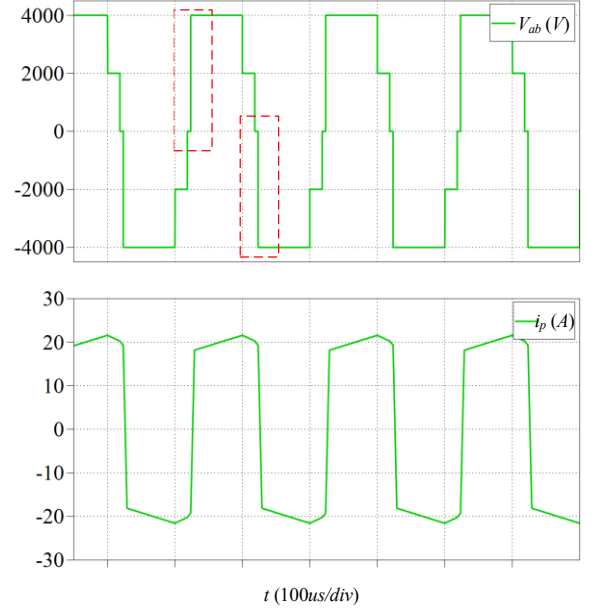
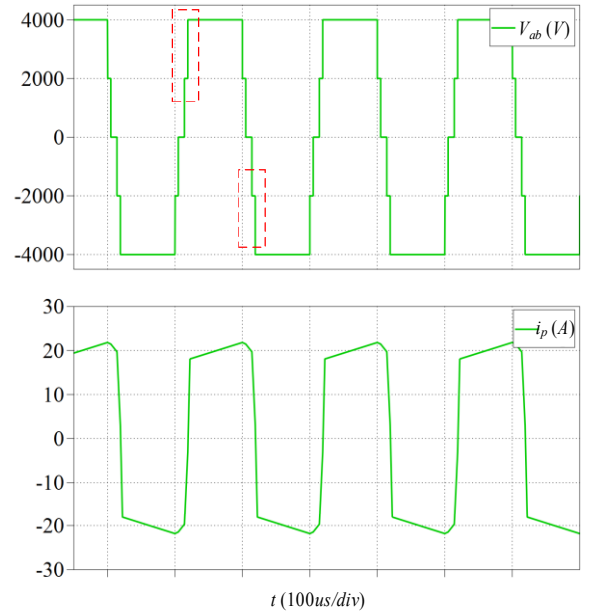


Fig. 3. Simulation results under the proposed control strategy including  $V_{in}$ ,  $V_{ab}$ ,  $V_o$ ,  $i_p$ ,  $i_{Lo}$ , and  $I_o$ .



(a)



(b)

Fig. 4. Comparison results including  $V_{ab}$  and  $i_p$ . (a) Under the control strategy in [14]. (b) Under the proposed control strategy.

#### V. CONCLUSION AND FUTURE WORK

In this paper, a double phase-shift control strategy is proposed for the FBTL dc/dc converter which is applied to dc distribution grids with the high dc bus voltage. By utilizing the proposed double phase-shift control strategy, the voltage change rate  $dv/dt$  and voltage stress on the transformer are

effectively reduced, which means the EMI and reliability of the converter can be improved. The operation principle and performance of the FBTL dc/dc converter under the proposed control strategy are analyzed in detail. Finally, a simulation model is built and simulation results validate the effectiveness and feasibility of the proposed control strategy.

#### APPENDIX

See Table I.

TABLE I. PARAMETERS OF THE SIMULATION MODEL

Component	Description
Turns Ratio of the Transformer $T_r (n : 1)$	4 : 1
Input Capacitors $C_1$ and $C_2$ ( $\mu\text{F}$ )	4700
Output Filter Inductor $L_o$ ( $\mu\text{H}$ )	1000
Output Filter Capacitor $C_o$ ( $\mu\text{F}$ )	4700
Input Voltage $V_{in}$ (kV)	4
Output Voltage $V_o$ (V)	800
$\alpha_c$ ( $\mu\text{s}$ )	5
Output Power (kW)	64
Switching Frequency (kHz)	5

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